

PATENT

Docket No:36856.00260

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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For: MULTILAYER CAPACITOR

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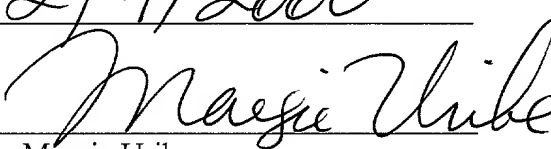
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2/9/2000

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MULTILAYER CAPACITOR

This application is a Continuation-in-Part of U.S. Patent Application No. 09/042,379 filed on March 13, 1998.

BACKGROUND OF THE INVENTION**1. Field of the Invention**

The present invention relates to a multi-layer capacitor and, more particularly, to a multi-layer capacitor which can be advantageously used in high frequency circuits.

2. Description of the Related Art

Conventional multi-layer capacitors include those described in Japanese Unexamined Patent Publication No. H2-256216 in which a multi-layer capacitor 1, as shown in Figs. 15 through 17 of the present application, is disclosed. Fig. 15 is a plan view of the external appearance of the multi-layer capacitor 1. Fig. 16 is a plan view of a first section of the multi-layer capacitor 1 showing a first electrode 10 located on one surface of one internal dielectric layer 9 of the capacitor 1. Fig. 17 is a plan view of a second section of the multi-layer capacitor 1 showing a second electrode 11 located on one surface of a differential internal dielectric layer 9 of the capacitor 1.

Referring to Figs. 15-17, the multi-layer capacitor 1 includes a capacitor main body 8 in the form of a rectangular parallelepiped having two principal surfaces 2 and 3 in a face-to-face relationship with each other and four side surfaces 4, 5, 6 and 7 connecting the principal surfaces 2 and 3. The capacitor main body 8 includes a plurality of dielectric layers 9 (Figs. 16-17) made of, for example, a ceramic dielectric material. Each of the dielectric layers is generally planar in shape and lies generally parallel to the principal surfaces 2 and 3. At least a pair of first and second internal electrodes 10 and 11 are provided on respective surfaces of the dielectric layers 9 in a

face-to-face relationship with each other, with a dielectric layer 9 interposed therebetween to form a capacitor unit.

The first internal electrode 10 is formed with four lead electrodes 12, 13, 14 and 15 which extend to two opposing side surfaces 4 and 6, as shown.

Each lead electrode 12, 13, 14 and 15 is coupled to a respective external terminal electrode 16, 17, 18 and 19 provided on the side surfaces 4 and 6 of the capacitor main body 8. Specifically, the lead electrodes 12 and 13 are connected to the external terminal electrodes 16 and 17, respectively, which are located on the side surface 4, and the lead electrodes 14 and 15 are connected to the external terminal electrodes 18 and 19, respectively, which are located on the side surface 6.

Referring to Fig. 17, the second internal electrode 11 is also formed with four lead electrodes 20, 21, 22 and 23 which extend to the side surfaces 4 and 6, respectively. More specifically, the lead electrodes 20 and 21 extend to positions on the side surface 4 which are different from the positions to which the lead electrodes 12 and 13 extend, and the lead electrodes 22 and 23 extend to positions on the side surface 6 of the main body 8 which are different from the positions to which the lead electrodes 14 and 15 extend.

The lead electrodes 20 through 23 are electrically coupled to external terminal electrodes 24, 25, 26 and 27, respectively. External terminal electrodes 24 and 25 are located on the side surface 4 at positions which are different from those of the external terminal electrodes 16 and 17. External terminal electrodes 26 and 27 are located on the side surface 6 at positions which are different from the positions of the external terminal electrodes 18 and 19.

Thus, the plurality of first external terminal electrodes 16 through 19 and the plurality of second external terminal electrodes 24 through 27 are arranged on the two side surfaces 4 and 6 such that they alternate adjacently to each other.

Fig. 18 illustrates current flowing through the multi-layer capacitor 1 as viewed in plan view corresponding to Fig. 17. In Fig. 18, first internal electrode 10 and second internal electrode 11, shown with broken and solid lines, respectively, are shown in an overlapping relationship.

In Fig. 18, the arrows indicate typical current paths and directions. In the state illustrated, current flows from each of the external terminal electrodes 24 through 27 to each of the external terminal electrodes 16 through 19. Because an alternating current is used, the direction of current flow will reverse periodically.

When the currents flow, magnetic flux is induced. The direction of the flux is determined by the direction of the currents to produce self-inductance components. Since the currents flow in various directions at central regions 28 (indicated by circles) of the internal electrodes 10 and 11, the induced magnetic flux generated by the various currents is canceled and substantially no net magnetic flux is produced in those regions.

The current in the vicinity of each of the external terminal electrodes 16 through 19 and 24 through 27 tends to flow toward each of the external terminal electrodes 16 through 19 and away from each of the external terminal electrodes 24 through 27. There are currents that flow to the left and right as viewed in Fig. 18 to spread at an angle of about 180 degrees. As a result, a major part of magnetic flux is canceled and there is no significant generation of net magnetic flux in these areas.

Therefore, in the multi-layer capacitor 1 shown in Figs. 15 through 17, the generation of self-inductance is suppressed in the areas points described above to reduce equivalent series induction (hereinafter "ESL").

However, currents flow substantially in the same direction in the vicinity of each of the side surfaces 5 and 7 on which no external terminal electrodes are provided, i.e., at each of the left and right edge portions indicated by hatching in Fig. 18. This results in substantially no cancellation of magnetic flux in these areas and significant net self-inductance is created. Therefore, the measures taken to reduce ESL in the multi-layer capacitor 1 shown in Figs. 15 through 17 are less than desirable.

SUMMARY OF THE INVENTION

To overcome the problems described above, preferred embodiments of the present invention provide a multi-layer capacitor which more effectively reduces ESL.

In accordance with a preferred embodiment the present invention, a multi-layer capacitor includes a capacitor body including top and bottom surfaces and opposed side surfaces which have continuously flat surfaces and are disposed between the top and bottom surfaces and opposed end surfaces disposed between the top and bottom surfaces and the opposed side surfaces, the capacitor body including a plurality of first electrode plates and a plurality of second electrode plates, the first and second electrode plates being interleaved with each other in opposed and spaced apart relation, a dielectric material located between each opposed set of the first and second electrode plates, the first and second electrode plates each including a main electrode portion and a plurality of spaced apart lead structures extending therefrom, respective lead structures of the first electrodes plates being located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement, and a plurality of electrical terminals located on each of the opposed side surfaces of the capacitor body, corresponding lead structures of the first electrode plates and corresponding lead structures of the second electrode plates being electrically connected together by respective ones of the electrical terminals to define a plurality of first polarity electrical terminals and a plurality of second polarity electrical terminals, respectively, located on the capacitor body; wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across the capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across the capacitor body and at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

Another preferred embodiment of the present invention provides a multi-layer capacitor including a capacitor body including a pair of opposed side surfaces having continuously smooth surfaces and a pair of opposed end surfaces disposed between the pair of opposed side surfaces, at least four electrical terminals disposed on each of the opposed side surfaces, the capacitor body also including at least one first electrode plate having a generally substantially rectangular first main electrode portion with a plurality of first lead structures extending therefrom and at least one second electrode

plate situated in opposed and spaced apart relation to the first electrode plate, the second electrode plate having a generally substantially rectangular second main electrode portion with a plurality of second lead structures extending therefrom, respective ones of the first lead structures being located adjacent respective ones of the second lead structures in an interdigitated arrangement and extending to respective ones of the electrical terminals; dielectric material disposed between each opposing set of first and second electrode plates, wherein each of the lead terminals of the at least one first electrode plate being disposed opposite to another of the lead terminals of the at least one first electrode plate across the capacitor body and each of the lead terminals of the at least one second electrode plate being disposed opposite to another of the lead terminals of the at least one second electrode plate across the capacitor body and at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

In other preferred embodiments based on the two preferred embodiments described above, it is preferred that the ratio L/W is equal to about 1.3 or less and equal to about 0.4 or greater.

Further, it is preferred that the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

In other preferred embodiments, lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

Also, it is preferred that the lengths L of all of the lead electrodes are substantially equal to each other.

The internal and lead electrodes are preferably arranged in such a manner that when currents of different polarity are applied to the first and second internal electrodes, the net induced inductance in the area of all four of the side surfaces is substantially zero.

In a preferred embodiment of the present invention, the first internal electrode is formed with at least four first lead electrodes which extend respectively to respective ones of the four side surfaces. An equal number of first external terminal electrodes are provided. At least one of the first external terminal electrodes is located on each of the four side surfaces.

In this preferred embodiment, the second internal electrode is formed with at least four second lead electrodes which extend to respective ones of the four side surfaces. An equal number of second external terminal electrodes are provided. At least one of the second external terminal electrodes is located on each of the four side surfaces.

It is more advantageous if the above-described configuration is used for both of the first and second internal electrodes.

In another preferred embodiment, for each side surface which has both a first and a second external terminal electrode, each of the first external terminal electrodes located on that surface is located adjacent to one a corresponding second external terminal electrode located on that side surface. It is more advantageous if all of the first external terminal electrodes and all of the second external terminal electrodes are arranged such that they alternate with each other throughout the four side surfaces.

In yet another preferred embodiment, all of the external terminal electrodes are arranged such that they are not adjacent to any other external electrode which is connected to the same internal electrode.

In still another preferred embodiment, the first internal electrode is formed with three first lead electrodes which extend respectively to three of the side surfaces. The second internal electrode is formed with two second lead electrodes which extend respectively to two of the side surfaces, one of which does have a first external electrode.

In another preferred embodiment, at least one of the first and at least one of the second external terminal electrodes is provided on each of the four side surfaces.

A plurality of capacitor units can be provided in the multi-layer capacitor. Each capacitor unit includes a respective pair of first and second internal electrodes with a respective dielectric layer located therebetween.

According to various preferred the present invention, the effect of reducing ESL can be expected from effective cancellation of magnetic and reduction of the lengths of currents achieved by providing a third internal electrode facing at least either the first or second internal electrodes with a dielectric material layer interposed therebetween. The third internal electrode is formed with at least two third lead electrodes which extend to respective ones of the side surfaces. An equal number of third external terminal electrodes are provided on the corresponding side surfaces and are electrically coupled to respective ones of the third lead electrode.

In the above-described preferred embodiment, when all of the first, second and third external terminal electrodes are arranged in the same order of arrangement repeated throughout the four side surfaces, the various components of magnetic flux can be more effectively canceled and the lengths of the current paths can be shortened further for a further reduction of ESL.

Other features, characteristics, elements and advantages of preferred embodiments of the present invention will be described in more detail below with reference to the figures attached hereto.

BRIEF DESCRIPTION OF THE DRAWINGS

For the purpose of illustrating the invention, there is shown in the drawing several forms which are presently preferred, it being understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown.

Fig. 1 is a plan view of a multi-layer capacitor 31 according to a first preferred embodiment of the present invention;

Fig. 2 is a plan view of the multi-layer capacitor 31 shown in Fig. 1 showing an internal structure thereof in the form of a section along which a first internal electrode 40 extends;

Fig. 3 is a plan view of the multi-layer capacitor shown 31 in Fig. 1 showing an internal structure thereof in the form of a section along which a second internal electrode 41 extends;

Fig. 4 is a plan view illustrating currents flowing in the multi-layer capacitor 31;

Fig. 5 is a plan view of a multi-layer capacitor 71 according to a second preferred embodiment of the invention showing the external appearance thereof;

Fig. 6 is a plan view of the multi-layer capacitor 71 shown in Fig. 5 showing an internal structure thereof in the form of a section along which a first internal electrode 40a extends;

Fig. 7 is a plan view of the multi-layer capacitor 71 shown in Fig. 5 showing an internal structure thereof in the form of a section along which a second internal electrode 41a extends;

Fig. 8 is a plan view of a multi-layer capacitor 81 according to a third preferred embodiment of the invention showing the external appearance thereof;

Fig. 9 is a plan view of the multi-layer capacitor 81 shown in Fig. 8 showing an internal structure thereof in the form of a section along which a third internal electrode 82 extends;

Fig. 10 is a plan view of the multi-layer capacitor 81 shown in Fig. 8 showing an internal structure thereof in the form of a section along which a first internal electrode 40b extends;

Fig. 11 is a plan view of the multi-layer capacitor 81 shown in Fig. 8 showing an internal structure thereof in the form of a section along which a second internal electrode 41b extends;

Fig. 12 is a plan view of a multi-layer capacitor 91 according to a fourth preferred embodiment of the invention showing the external appearance thereof;

Fig. 13 is a plan view of the multi-layer capacitor 91 shown in Fig. 12 showing an internal structure thereof in the form of a section along which a first internal electrode 40c extends;

Fig. 14 is a plan view of the multi-layer capacitor 91 shown in Fig. 12 showing an internal structure thereof in the form of a section along which a second internal electrode 41c extends;

Fig. 15 is a plan view of a conventional multi-layer capacitor 1 which is of interest to the present invention showing the external appearance thereof;

Fig. 16 is a plan view of the multi-layer capacitor 1 shown in Fig. 15 showing an internal structure thereof in the form of a section along which a first internal electrode 10 extends;

Fig. 17 is a plan view of the multi-layer capacitor 1 shown in Fig. 15 showing an internal structure thereof in the form of a section along which a second internal electrode 11 extends;

Fig. 18 is a plan view illustrating currents flowing in the multi-layer capacitor 1 shown in Fig. 15;

Fig. 19 is a plan view of a multi-layer capacitor 101 according to a fifth preferred embodiment of the present invention;

Fig. 20 is a plan view of the multi-layer capacitor 101 shown in Fig. 19 showing an internal structure thereof in the form of a section along which a first internal electrode 40d extends; and

Fig. 21 is a plan view of the multi-layer capacitor 101 shown in Fig. 10 showing an internal structure thereof in the form of a section along which a second internal electrode 41d extends.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

First Preferred Embodiment

Referring now to the drawings, wherein like numerals indicate like elements, there is shown in Figs. 1 through 3 a first preferred embodiment of a multi-

layer capacitor constructed in accordance with the principles of the present invention and designated generally as 31. Figs. 1 through 3 correspond to Figs. 15 through 17.

Fig. 1 is a plan view of the external appearance multi-layer capacitor 31. Fig. 2 is a plan view multi-layer capacitor 31 showing a first internal electrode 40 located on one surface of a first internal dielectric layer 39 of the capacitor 31. Fig. 3 is a plan view of a second section of the multi-layer capacitor 31 showing a second internal electrode 41 located on one surface of a second internal dielectric layer 39 of the capacitor 31.

Multi-layer capacitor 31 includes a capacitor main body 38 in the form of a rectangular parallelepiped having two opposed principal surfaces 32 and 33 and four side surfaces 34, 35, 36 and 37 extending therebetween. The capacitor main body 38 includes a plurality of generally planar dielectric layers 39 made of, for example, a ceramic dielectric material. The main surfaces of the dielectric layers 39 are situated generally parallel to the principal surfaces 32, 33 of the capacitor main body 38. At least a pair of first and second internal electrodes 40 and 41 are provided in a face-to-face relationship with each other with a dielectric material layer 39 interposed therebetween, each such pair of internal electrodes forming a respective capacitor unit.

As shown in Fig. 2, the first internal electrode 40 has six lead electrodes 42, 43, 44, 45, 46 and 47, each of which extends to a respective one of the four side surfaces 34 through 37. Particularly, the lead electrodes 42 and 43 extend to the side surface 34; the lead electrode 44 extends to the side surface 35; the lead electrodes 45 and 46 extend to the side surface 36; and the lead electrode 47 extends to the side surface 37.

Each lead electrode 42-47 is electrically coupled to a respective external terminal electrodes 48-53. The external terminal electrodes 48 and 49, connected to the lead electrodes 42 and 43, respectively, are located on the side surface 34; the external terminal electrode 50, connected to the lead electrode 44, is located on the side surface 35; the external terminal electrodes 51 and 52, connected to the lead electrodes 45 and 46, respectively, are located on the side surface 36; and the external

terminal electrode 53, connected to the lead electrode 47, is located on the side surface 37.

As shown in Fig. 3, the internal electrode 41 is formed with six second lead electrodes 54, 55, 56, 57, 58 and 59, each of which extends to a respective one of the four side surfaces 34 through 37. More specifically, the lead electrodes 54 and 55 extend to side surface 34; lead electrode 56 extends to side surface 35; lead electrodes 57 and 58 extend to side surface 36; and lead electrode 59 extends to the side surface 37.

The positions on the side surfaces 34 through 37 to which the respective lead electrodes 54 through 59 extend are different from the positions to which the respective lead electrodes 42 through 47 extend.

External terminal electrodes 60, 61, 62, 63, 64 and 65, which are electrically coupled to respective lead electrodes 54 through 59, are provided on the side surfaces 34 through 37 at positions which are different than the positions of the external terminal electrodes 48 through 53. External terminal electrodes 60 and 61, connected to lead electrodes 54 and 55, respectively, are located on side surface 34; external terminal electrode 62, connected to lead electrode 56, is located on side surface 35; external terminal electrodes 63 and 64, connected to lead electrodes 57 and 58, respectively, are located on side surface 36; and external terminal electrode 65, connected to lead electrode 59, are located on side surface 37.

The external terminal electrodes 48 through 53 are arranged in an interleaved manner such that no two external electrodes which are electrically coupled to the same internal electrode 40 or 41 are adjacent one another. In operation, the polarizations of the first and second internal electrodes 40, 41 are preferably opposite to one another.

In order to increase the capacity of the multi-layer capacitor 31, additional pairs of internal electrodes can be provided to define additional capacitor units. For example, the multi-layer capacitor 31 can include two sets of capacitor units, each set being defined by a respective pair of first and second internal electrodes 40, 41 separated by a respective dielectric layer. The plurality of capacitor units are preferably

connected in parallel by at least either appropriate ones of the first external terminal electrodes 48 through 53 or the second external terminal electrodes 60 through 65.

Each of the external terminal electrodes 48 through 53 and 60 through 65 is preferably formed so as to extend not only on the side surfaces 34 through 37 but also onto a part of each of the principal surfaces 32 and 33.

Fig. 4 illustrates various currents, flowing in the multi-layer capacitor 31. In Fig. 4, the first internal electrode 40 is indicated by a broken line and the second internal electrode 41 is indicated by a solid line, the two electrodes being illustrated in an overlapping relationship.

As apparent from these typical paths and the directions of current flow indicated by the arrows in Fig. 4 (the direction of current flow indicates that direction of each of the noted current paths at a given point in time, the direction of the flow of current through these paths will alternate periodically), a current flows from each of the second external terminal electrodes 60 through 65 to each of the first external terminal electrodes 48 through 53. When such currents flow, induced magnetic flux is generated.

As in the prior art, the various components of the induced flux at the central regions 66 indicated by the circles cancel one another out because currents flow in various directions. Similarly, the various components of the induced flux in the areas of the side surfaces 34 and 36 tend to cancel one another. In this connection, current flow in the area of side surfaces 34 and 36 is very similar to that of the prior art of Fig. 18.

However, the embodiment of Figs. 1-4 produces a much more desirable result in the areas 67 adjacent the side surfaces 35, 37. Since the first external terminal electrodes 50 and 53 and the second external terminal electrodes 62 and 65 are provided at the side surfaces 34 and 36, there is no significant net current flow in the areas 67 and no significant generation of net magnetic flux.

As a result, the degree of net induced magnetic flux generated over the entire region of the multi-layer capacitor 31 is significantly reduced, thereby allowing the ESL to be suppressed to a very low level.

Another advantage of this embodiment is that the current paths between each of the electrodes is reduced. Particularly, each of the first lead electrodes 42 through 47 (and the first external terminal electrodes 48 through 53) is located relatively close to its adjacent second lead electrode 54 through 59 (and the second external terminal electrode 60 through 64) compared to the prior art of Fig.18. This reduces the lengths of the current paths and thereby reduces self-inductance components produced between them.

Second Preferred Embodiment

Figs. 5 through 7 show a multi-layer capacitor 71 according to a second preferred embodiment of the present invention. Fig. 5 is a plan view of the external appearance of the multi-layer capacitor 71. Fig. 6 is a plan view showing one surface of an internal dielectric layer 39 of the multi-layer capacitor 71 having a first internal electrode 40a located thereon. Fig. 7 is a plan view showing one surface of a different one of the internal dielectric layers 39 of the multi-layer capacitor 71 having a second internal electrode 41a located thereon.

Figs. 5 through 7 respectively correspond to Figs. 1 through 3 of the first preferred embodiment. In Figs. 5 through 7, elements corresponding to elements shown in Figs. 1 through 3 are indicated by like reference numbers and will not be described here to avoid duplication.

Referring to Fig. 6, the first internal electrode 40a is formed with five lead electrodes 42, 43, 45, 46 and 47a which extend to respective side surfaces 34, 36 and 37. The multi-layer capacitor 71 is different from the multi-layer capacitor 31 of the first embodiment in that the multi-layer capacitor 71 has no lead electrode extending to side surface 35. Additionally, lead electrode 47a extends to the middle of the side surface 37, whereas lead electrode 47 extends to the upper half of side surface 37.

The five lead electrodes 42 through 47a are electrically coupled to five external terminal electrodes 48, 49, 51, 52 and 53a, respectively. The five external electrodes 48, 49, 51, 52 and 53a, are each located on one of the three side surfaces 34, 36 and 37. The multi-layer capacitor 71 is different from the multi-layer capacitor 31

of the first preferred embodiment in that the multi-layer capacitor 71 has no external terminal corresponding to the first external terminal electrode 50 and in that the external terminal electrode 53a is different in location from the external terminal electrode 53.

Referring to Fig. 7, a second internal electrode 41a has five lead electrodes 54, 55, 56a, 57 and 58 which extend to respective side surfaces 34 through 36. The multi-layer capacitor 71 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it has no lead electrode extending to the side surface 37 and in that the lead electrode 56a which extends to the side surface 35 extends to the middle of the side surface 35, rather than the bottom of the side surface 35 as is the case with lead electrode 56 of the first preferred embodiment.

Each of the lead electrodes 54 through 58 is electrically coupled to a respective external terminal electrode 60, 61, 62a, 63 and 64. Each of these terminal electrodes are provided on a respective side surface 34 through 36. The multi-layer capacitor 71 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it has no external terminal corresponding to the external terminal electrode 65 and in that the external terminal electrode 62a is located in a different position than the external terminal electrode 62.

If desired, the capacity of multi-layer capacitor 71 can be increased by providing a plurality of capacitive units, each defined by a respective set of internal electrodes 40a, 41a, separated by a respective dielectric layer 38. The plurality of capacitor units are then connected in parallel by appropriate ones of the external terminal electrodes 48 through 53a or 60 through 64.

In the second preferred embodiment of the invention, each of the external terminal electrodes 48, 49, 51 and 52 coupled to the first internal electrode 40a is located adjacent to at least one of the external terminal electrodes 60, 61, 63 and 64 coupled to internal electrode 41a. Further, only the second external terminal electrode 62a is located on the side surface 35, and only the first external terminal electrode 53a is located on the side surface 37. By providing the external terminal electrodes 62a and 53a on the side surfaces 35 and 37, respectively, it is possible to direct the flow of the currents on the internal electrodes 40a and 41a in various directions to achieve a level

of cancellation of magnetic flux that is higher than that which is achievable in the conventional multi-layer capacitor 1 shown in Figs. 15 through 17. It is also possible to reduce the length of the path of these currents thereby further reducing the induced inductance components.

Third Preferred Embodiment

Figs. 8 through 11 show a multi-layer capacitor 81 according to a third preferred embodiment of the present invention. Fig. 8 is a plan view of the external appearance of the multi-layer capacitor 81. Fig. 9 is a plan view of the surface of one of the internal dielectric layers 39 of the multi-layer capacitor 81 having a first internal electrode 82 formed thereon. Fig. 10 is a plan view of the surface of one of the internal dielectric layers 39 of the multi-layer capacitor 81 having a second internal electrode 40b formed thereon. Fig. 11 is a plan view of the surface of one of the internal dielectric layers 39 of the multi-layer capacitor 81 having a third internal electrode 41b formed thereon.

In Figs. 8 through 11, elements corresponding to elements shown in Figs. 1 through 3 are indicated by like reference numbers and will not be described here to avoid duplication.

The multi-layer capacitor 81 of the third preferred embodiment of the invention includes a third internal electrode 82 facing at least either the first internal electrode 40b or second internal electrode 41b with a dielectric material layer 39 interposed therebetween. The third internal electrode 82 is formed with four lead electrodes 83, 84, 85 and 86, each of which extends to a respective side surface 34 and 36. More specifically, lead electrodes 83 and 84 extend to side surface 34, and lead electrodes 85 and 86 extend to side surface 36.

External terminal electrodes 87, 88, 89 and 90, which are electrically coupled to the lead electrodes 83 through 86, respectively, are provided on respective side surfaces 34 and 36. The multi-layer capacitor 81 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it includes the third external terminal electrodes 87 and 90 provided, respectively, in the positions where the first

external terminal electrodes 48 and 52 are provided on the multi-layer capacitor 31 of the first embodiment and includes the third external terminal electrodes 88 and 89 provided respectively in the positions where the second external terminal electrodes 61 and 63 are provided on the multi-layer capacitor 31.

Referring to Fig. 10, a first internal electrode 40b has four first lead electrodes 42b, 44, 45b and 47 which extend to respective side surfaces 34 through 37. The first internal electrode 40b of the multi-layer capacitor 81 is different from the multi-layer capacitor 31 of the first embodiment in that it has only one lead electrode 42b which extends to side surface 34 and one lead electrode 45b which extends to side surface 36.

Four first external terminal electrodes 48b, 50, 51b and 53 are electrically coupled to the four first lead electrodes 42b through 47, respectively, and are provided on the four side surfaces 34 through 37, respectively. The multi-layer capacitor 81 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it includes the first external terminal electrodes 48b and 51b provided respectively in the positions where the second external terminal electrodes 60 and 64 are provided on the multi-layer capacitor 31.

Referring to Fig. 11, a second internal electrode 41b has four second lead electrodes 54b, 56, 57b and 59 which extend to respective side surfaces 34 through 37. The second internal electrode of the multi-layer capacitor 81 is different from the second internal electrode 41 of the multi-layer capacitor 31 of the first preferred embodiment in that only one lead electrode 54b extends to the side surface 34 and only one lead electrode 57b extends to side surface 36.

Four second external terminal electrodes 60b, 62, 63b and 65 are electrically coupled to the four first lead electrodes 54b through 59, respectively. The four second external terminal electrodes are provided on the four side surfaces 34 through 37, respectively. The multi-layer capacitor 81 is different from the multi-layer capacitor 31 of the first preferred embodiment in that the second external terminal electrodes 60b and 63b provided, respectively, in the positions where the first external terminal electrodes 49 and 51 are provided on the multi-layer capacitor 31.

By way of example, the multi-layer capacitor 81 can be formed by locating the third internal electrode 82, the first internal electrode 40b and the second internal electrode 41b, one above the other with respective dielectric layers being located therebetween. Irrespective of the relative locations of the internal electrodes, the external terminal electrodes are arranged such that each of the third external terminal electrodes 87 through 90 is followed by one of the first external terminal electrodes 48b through 53 and then followed by one of the second external terminal electrodes 60b through 65. This alternating arrangement is repeated throughout the four side surfaces 34 through 37. The above-described order of stacking the internal electrodes 82, 40b and 41b may be changed arbitrarily.

In order to increase the capacity of the multi-layer capacitor 81, a plurality of third internal electrodes 82, first internal electrodes 40b and second internal electrodes 41b may be provided to form a plurality of capacitor units. For example, a plurality of third internal electrodes 82 and a plurality of first internal electrodes 40b may be provided; a plurality of second internal electrodes 41b and a plurality of third internal electrodes 82 may be provided; or a plurality of third internal electrodes 82, a plurality of first internal electrodes 40b and a plurality of second internal electrodes 41b may be provided. The resultant capacitor units are connected in parallel by at least any of the third external terminal electrodes 87 through 90, the first external terminal electrodes 48b through 53 and the second external terminal electrodes 60b through 65.

Like the first preferred embodiment, external terminal electrodes connected to different internal electrodes (that is, external terminal electrodes having different polarities) are located on each of the four side surfaces 34 through 37. More specifically, first external terminal electrode 48b, second external terminal electrode 60b and third external terminal electrodes 87 and 88 are located on the side surface 34; first external terminal electrode 50 and second external terminal electrode 62 are located on side surface 35; first external terminal electrode 51b, second external terminal electrode 63b and third external terminal electrodes 85 and 90 are located on side surface 36; and first external terminal electrode 53 and second external terminal electrode 65 are located on side surface 37.

Therefore, according to the third preferred embodiment of the invention, since the flow of currents on the internal electrodes 40b and 41b can be directed in various directions to effectively cancel magnetic flux and to reduce the lengths of the current paths, the induced inductance components can be reduced.

Although the arrangement of the third preferred embodiment is different from that in the first preferred embodiment in that external terminal electrodes having different polarities are not necessarily adjacent to each other in all locations, the directions of the current flows on the internal electrodes 40b and 41b is more diverse than those in the conventional multi-layer capacitor 1 shown in Figs. 15 through 17 and the lengths of the current paths are shorter. This makes it possible to achieve a higher reduction of the induced inductance components.

As an alternative to the third preferred embodiment, a multi-layer capacitor may be provided in which only the first and second internal electrodes 40b and 41b are provided and the third internal electrode 82 is excluded. Further, the third internal electrode 82 may be formed with lead electrodes which extend to the side surfaces 35 and 37.

Fourth Preferred Embodiment

Figs. 12 through 14 show a multi-layer capacitor 91 according to a fourth preferred embodiment of the present invention. Fig. 12 is a plan view of the external appearance of the multi-layer capacitor 91. Fig. 13 is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor 91 having a first internal electrode 40c formed thereon. Fig. 14 is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor 91 having a second internal electrode 41c formed thereon.

Figs. 12 through 14 respectively correspond to Figs. 1 through 3 of the first preferred embodiment. In Figs. 12 through 14, elements corresponding to elements shown in Figs. 1 through 3 are indicated by like reference numbers and will not be described here to avoid duplication.

The multi-layer capacitor 91 of the fourth preferred embodiment of the invention resembles the multi-layer capacitor 71 of the second embodiment in its

external appearance. A first internal electrode 40c has five first lead electrodes 42, 43, 44c, 45c and 46c which extend to respective side surfaces 34, 35 and 36. The multi-layer capacitor 91 is different from the multi-layer capacitor 31 of the first preferred embodiment in that does not include a lead electrode corresponding to the lead electrode 47 which extends to the side surface 37 and in that the positions at which the lead electrodes 44c, 45c and 46c respectively extends to the side surfaces 35 and 36 are different from the positions that the lead electrodes 44 through 46 extend to those surfaces.

Five external terminal electrodes 48, 49, 50c, 51c and 52c are electrically coupled to the five lead electrodes 42 through 46c, respectively. These external electrodes are provided on the side surfaces 34 through 36. The multi-layer capacitor 91 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it does not include an external terminal electrode corresponding to the first external terminal electrode 53 and in that the positions of the external terminal electrodes 50c, 51c and 52c are different from the positions of the external terminal electrodes 50 through 52, respectively.

Referring to Fig. 14, a second internal electrode 41c has five lead electrodes 54, 55, 57c, 58c and 59c, each of which extends to a respective side surfaces 34, 36 and 37. The multi-layer capacitor 91 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it does not include a lead electrode corresponding to the lead electrode 59 which extends to the side surface 35 and in that the positions of the lead electrodes 57c, 58c and 59c are different from the positions of the lead electrodes 57 through 59, respectively.

The external terminal electrodes 60, 61, 63c, 64c and 65c which are electrically coupled to second lead electrodes 54 through 59c, respectively, are provided on the side surfaces 34, 36 and 37. The multi-layer capacitor 91 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it does not include an external terminal electrode corresponding to the second external terminal electrode 62 and in that the positions of the external terminal electrodes 63c, 64c and

65c are different from the positions of the external terminal electrodes 63 through 65, respectively.

In order to increase the capacity of multi-layer capacitor 91, a plurality of first internal electrodes 40c and a plurality of second internal electrodes 41c can be provided. Pairs of internal electrodes 40c, 41c will face one another with a dielectric layer formed therebetween so as to form respective capacitor units. These capacitor units will be connected in parallel by at least either the first external terminal electrodes 48 through 52c or the second external terminal electrodes 60 through 65c.

Like the first preferred embodiment described above, each of the first external terminal electrodes 48 through 52c of the fourth preferred embodiment of the invention is arranged so as to alternate with respective ones of the second external terminal electrodes 60 through 65c throughout the four side surfaces 34 through 37. The fourth preferred embodiment is different from the second preferred embodiment in this regard.

Therefore, according to the fourth preferred embodiment of the invention, since the flow of currents on the internal electrodes 40c and 41c can be directed in various directions, the various components of induced magnetic flux will be cancelled and the lengths of the current paths will be shortened relative to the prior art of Figs. 15-17. The fourth preferred embodiment will effectively reduce the induced inductance components to a degree which is similar to that of the first preferred embodiment.

In relation to additional features and advantages of the fourth preferred embodiment, the inventors discovered that variations in dimensions and relationships between such dimensions of the lead electrodes materially affect the ESL of the capacitors of the fourth preferred embodiment and each of other preferred embodiments described herein. These further features and advantages described in the following paragraphs are shown as being incorporated in the fourth preferred embodiment of Figs. 12-14 but can be applied and incorporated in any of the preferred embodiments disclosed herein.

More specifically, the length and the width of a lead-out portion are designated by reference characters L, W in FIG. 13, for example. In each of the above-

described preferred embodiments, currents in the main portions of the first internal electrodes and the second internal electrodes flow in different directions, so that the generation of a magnetic flux is prevented. However, in the respective lead electrodes, currents flow in a uniform direction. Therefore, a magnetic flux is generated, and an inductance is generated in accordance with the magnetic flux. Further, the state of currents flowing in the respective main portions of the first internal electrodes and the second internal electrodes is changed, depending on the lengths and the widths of the lead electrodes. Accordingly, the lengths and the widths of the lead electrodes significantly affect the ESL value of the capacitor.

To confirm the discovery described above, the lengths L and the widths W of all of the lead electrodes were varied in a multi-layer capacitor 91 according to a fourth preferred embodiment as shown in FIGS. 12 through 14. The capacitor 91 preferably includes a total of 10 lead electrodes, for example, in which four lead electrodes 42, 43, 54, 55 and four lead electrodes 45c, 46c, 57c, 58c are extended onto the side surfaces 34, 36, respectively, and moreover, and one lead electrode 44c and one lead electrode 59c are extended onto the side surfaces 35, 37, correspondingly.

TABLE 1 shows the results.

TABLE 1

	L=0. 1 mm	L=0. 2 mm	L=0. 3 mm	L=0. 5 mm
W=0. 08 mm	38 pH	65 pH	87 pH	106 pH
W=0. 16 mm	28 pH	35 pH	50 pH	81 pH
W=0. 24 mm	25 pH	32 pH	39 pH	58 pH

The numerical values listed in TABLE 1 are measurement values of the ESL obtained by a conventional publicly-known resonance method. As seen in the results, in the capacitors having plural lead electrodes, the ESL value is changed according to the ration of L/W. When the ratio L/W of the capacitors is about 3 or lower, the ESL value is less than about 80 pH. When the ratio L/W is about 1.3 or lower, the ESL value is less than about 40 pH.

In the above-described preferred embodiments, the widths of all of the plural lead electrodes are preferably substantially equal to each other. However, the above-described preferred range of the L/W value can be applied to capacitors having the structure in which the width of at least one of the lead electrodes is different from that of the respective remaining lead electrode(s). For example, this will be described in reference to FIGS. 13 and 14. The above-described preferred range of the L/W value can be applied to capacitors each having the structure in which the widths of one lead electrode 44c and one lead electrode 59c extending onto the side surfaces 35, 37, correspondingly, are wider as compared with four lead electrodes 42, 43, 54, 55 and four lead electrodes 45c, 46c, 57c, 58c extending onto the side surfaces 34, 36, respectively.

According to another preferred embodiment, a capacitor structure is similar to that of the multi-layer capacitor 91 according to the fourth preferred embodiment as shown in FIGS. 12 through 14, except that the lead electrodes 44c, 59c are not provided. The lengths L and the widths W of all the lead electrodes of this preferred embodiment were also varied to provide further confirmation of the discovery with respect to the ratio L/W described above. In this capacitor, four lead electrodes are preferably extended onto the side surfaces 34, 36, respectively. That is, the capacitor has a total of 8 lead electrodes, for example. TABLE 2 shows the results.

TABLE 2

	L=0. 1 mm	L=0. 2mm	L=0. 3 mm	L=0. 5 mm
W=0.08 mm	79 pH	107 pH	131 pH	176 pH
W=0.16 mm	68 pH	76 pH	95 pH	133 pH
W=0.24 mm	55 pH	66 pH	77 pH	106 pH

The numerical values in TABLE 2 are measurement values of ESL obtained by a conventional publicly-known resonance method. In this capacitor, when the ratio L/W is about 3 or lower, the ESL value is about 120 pH or lower. When the ratio L/W is about 1.3 or lower, the ESL value is about 80 pH or lower. For the prior art

structure described in the specification of this application, the same results are obtained.

In the above preferred embodiment, the widths of all the lead electrodes are preferably made substantially equal to each other. However, the above-described preferred range of the ratio L/W value can be applied to capacitors having the structure in which the width of at least one of the lead electrodes is wider than that of the respective remaining lead electrodes.

In recently developed microprocessing units (MPU), the operating frequency of nearly 1 GHz is to be used. Such an MPU contains an MPU chip and a capacitor. Capacitors combined with the MPU chip are required to have an ESL value of less than about 10 pH. If one capacitor can not satisfy the requirement, plural capacitors are connected in parallel. For the purpose of reducing an inductance component caused by the wiring being short-circuited between the plural capacitors and the MPU chip, the capacitors are arranged close to the four sides of the MPU chip. In the case that the total ESL value of the plurality of capacitors is less than about 10 pH, and one capacitor is arranged on each of the four sides of the MPU chip, it is required to provide capacitors each having an ESL value of less than about 40 pH. When two capacitors are arranged on each of the four sides of the MPU chip, it is required for each capacitor to have an ESL value of less than about 80 pH. When three capacitors are arranged on each of the four sides of a MPU chip, it is required for each capacitor to have an ESL value of less than about 120 pH. The L/W values which have been included in the above preferred embodiment are significant for providing capacitors satisfying such a requirement.

Accordingly, in preferred embodiments of the present invention, when the ratio L/W is about 3 or lower, low ESL capacitors which are practically useful can be obtained. Preferably, the ratio L/W is about 1.3 or lower. In general, when lead electrodes are widened, currents can flow smoothly from the portions of capacitors where charges are accumulated, that is, the respective main portions of the first internal electrodes and the second internal electrodes into the lead electrodes. However, preferably, the ratio L/W is about 0.4 or higher because when the ratio L/W is less than

about 0.4, the lengths of lead electrodes are short and/or the widths are wide, and therefore, deterioration of the electrical insulation and moisture-proof properties occurs.

Further, another preferred embodiment is arranged such that the outside dimensions of all of the first internal electrodes and all of the second internal electrodes are preferably substantially equal to each other, and the lengths of all the lead electrodes are preferably substantially equal to each other. In this preferred embodiment, the lengths of all of the lead electrodes are preferably substantially equal, and moreover can be reduced as much as possible. The static capacitance can be also made as large as possible.

On the other hand, when the outside dimensions of the first internal electrodes are smaller than those of the second internal electrodes, for example, the lengths of the lead electrodes connected to the first internal electrodes become relatively longer as compared with those of the second internal electrodes. Then, the ESL value is increased, as compared with that in the preferred embodiments of the present application. In other words, the capacitors of the preferred embodiments of this application have a much lower ESL value than capacitors having the structure in which the outside dimensions of the first internal electrodes and those of the second internal electrodes are different from each other.

Fifth Preferred Embodiment

Figs. 19 through 21 show a multi-layer capacitor 101 according to a fifth preferred embodiment of the present invention. Fig. 19 is a plan view of the external appearance of the multi-layer capacitor 101. Fig. 20 is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor 101 having a first internal electrode 40d formed thereon. Fig. 21 is a plan view of the surface of one of the dielectric layers of the multi-layer capacitor 101 having a second internal electrode 41d formed thereon.

Figs. 19 through 21 respectively correspond to Figs. 1 through 3 of the first preferred embodiment. In Figs. 19 through 21, elements corresponding to elements shown in Figs. 1 through 3 are indicated by like reference numbers and will not be described here to avoid duplication.

Referring to Fig. 20, a first internal electrode 40d has three first lead electrodes 44d, 45d and 47d which extend to respective side surfaces 35, 36 and 37. The multi-layer capacitor 101 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it does not include lead electrodes 42 and 43 which extend to the side surface 34, does not include a lead electrode 46 which extends to the side surface 36, and in that the positions at which the lead electrodes 44d, 45d, and 47d respectively extend to the side surfaces 35, 36 and 37 are different from the positions that the lead electrodes 44, 45 and 47 extend to those surfaces.

The three lead electrodes 44d, 45d and 47d are electrically coupled to three external terminal electrodes 50d, 51d and 53d respectively. These external terminal electrodes are provided on the side surfaces 35 through 37. The multi-layer capacitor 101 is different from the multi-layer 31 of the first preferred embodiment in that it does not include external terminal electrodes corresponding to the first external terminal electrodes 48, 49 and 52 in that the positions of the external terminal electrodes 50d, 51d and 53d are different from the positions of the external terminal electrodes 50, 51 and 53, respectively.

Referring to Fig. 21, a second internal electrode 41d has two lead electrodes 54d and 57d, each of which extends to respective side surfaces 34 and 36. The multi-layer capacitor 101 is different from the multi-layer capacitor 31 of the first preferred embodiment in that it does not include lead electrodes corresponding to the lead electrodes 61, 62, 64 and 65 which extends to the side surfaces 34 through 37, respectively, and in that the positions of the lead electrodes 54d and 57d are different from the positions of the lead electrodes 54 and 57, respectively.

Two external terminal electrodes 60d and 63d are electrically coupled to the two lead electrodes 54d and 57d, respectively, and are provided on the side surfaces 34 and 36. The multi-layer capacitor is different from the multi-layer capacitor 31 of the first preferred embodiment in that it does not include external terminal electrodes corresponding to the second external terminal electrodes 61, 62, 64 and 65, and in that the positions of the external terminal electrodes 60d and 63d are different from the positions of the external terminal electrodes 60 and 63, respectively.

In order to increase the capacity of multi-layer capacitor 101, a plurality of first internal electrodes 40d and a plurality of second internal electrodes 41d can be provided. Therefore, according to the fifth preferred embodiment of the invention, since the flow of the currents on the internal electrodes 40b and 41b can be directed in various directions to effectively cancel magnetic flux and to reduce the lengths of the current paths, the induced inductance components can be reduced.

Although the arrangement of the fifth preferred embodiment is different from that in that first preferred embodiment in that external terminal electrodes having different polarities are not necessarily adjacent to each other in all locations the directions of the current flows on the internal electrodes 40d and 41d is more diverse than those in the conventional multi-layer capacitor 1 shown in Figs. 15 and 17 and the lengths of the current paths are shorter. Therefore, this makes it possible to achieve a higher reduction of the induced inductance components.

Test Results

A sample of each of the multi-layer capacitor 31 according to the first preferred embodiment (preferred embodiment 1), the multi-layer capacitor 71 according to the second preferred embodiment (preferred embodiment 2), the multi-layer capacitor 81 according to the third preferred embodiment (preferred embodiment 3), the multi-layer capacitor 91 according to the fourth preferred embodiment (preferred embodiment 4) and the conventional multi-layer capacitor 1 (comparative example) was fabricated and ESL of each of them was evaluated.

Each sample was formed with outer plan dimensions of 3.2 mm X 2.5 mm. For samples having six layers of internal electrodes in total, i.e., those having two kinds of internal electrodes such as the multi-layer capacitors 31, 71, 91 and 1 (embodiments 1, 2 and 4 and comparative example), the stacking of the two kinds of internal electrodes was repeated three times (i.e., three pairs of internal electrodes were used to form three capacitance units). For the sample having three kinds of internal electrodes, i.e., the multi-layer capacitor 81 (preferred embodiment 3), the stacking of the three kinds of internal electrodes was repeated twice.

ESL was obtained using the resonance method. The resonance method is a method wherein the impedance frequency characteristics of each of the sample multi-layer capacitor is measured and ESL is obtained from a frequency f_0 at a minimum point (referred to as series resonance point between the capacity component C_s and ESL of the capacitor) using the following equation.

$$ESL = 1 / [(2\pi f_0)^2 \times C_s]$$

The measured value of ESL of each sample is shown in the Table 3 below.

Table 3

	ESL Value (pH)
Embodiment 1	40
Embodiment 2	72
Embodiment 3	85
Embodiment 4	51
Comparative Example	95

It is apparent from Tables 1-3 that ESL was suppressed to a greater degree in the examples of preferred embodiment 4, especially those in Table 1. Also, preferred embodiment 1 produced lower ESL values than the examples in Table 2 of preferred embodiment 4 and than the preferred embodiments 2 and 3

While the present invention has been described with reference to the illustrated preferred embodiments, for example, it is possible to change positions and the number of the lead-out electrodes of the internal electrodes variously and to change the positions and number of the external terminal electrodes accordingly within the scope of the invention.

As described above, according to the preferred embodiments of the present invention, at least either a first or a second internal electrode is formed with at least three lead electrodes which extend respectively to at least three of the side surfaces of a capacitor main body, and external terminal electrodes which are

electrically coupled to respective lead electrodes are provided on respective side surfaces. As a result, since the flow of currents on the internal electrodes can be directed in various directions to cancel magnetic flux and to reduce the lengths of the currents path effectively, ESL can be reduced.

With this structure, a high resonance frequency can be achieved and the frequency band of the capacitor can be increased. Accordingly, a multi-layer capacitor according to the invention can accommodate electronic circuits at higher frequencies than was possible with the comparative example and can be advantageously used, for example, as a bypass capacitor or decoupling capacitor in a high frequency circuit. Further, while a decoupling capacitor used in an MPU (microprocessing unit) must also have the function of a quick power supply (a function of supplying power from an amount of electricity charged in the capacitor when there is a sudden need for power as in the case of power-up), a multi-layer capacitor according to the invention can be used for such an application because it has low ESL.

In the preferred embodiments of the present invention below, the cancellation of magnetic fluxes as described above is further improved and the lengths of currents are further reduced to achieve more effective reduction of ESL.

It should be understood that the foregoing description is only illustrative of the invention. Various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention is intended to embrace all such alternatives, modifications and variances which fall within the scope of the appended claims.

What it is claimed is:

1. A multi-layer capacitor device comprising:

a capacitor body including top and bottom surfaces and opposed side surfaces which have continuously flat surfaces and are disposed between the top and bottom surfaces and opposed end surfaces disposed between the top and bottom surfaces and the opposed side surfaces, the capacitor body including a plurality of first electrode plates and a plurality of second electrode plates, the first and second electrode plates being interleaved with each other in opposed and spaced apart relation;

a dielectric material located between each opposed set of the first and second electrode plates;

the first and second electrode plates each including a main electrode portion and a plurality of spaced apart lead structures extending therefrom, respective lead structures of the first electrodes plates being located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement; and

a plurality of electrical terminals located on each of the opposed side surfaces of the capacitor body, corresponding lead structures of the first electrode plates and corresponding lead structures of the second electrode plates being electrically connected together by respective ones of the electrical terminals to define a plurality of first polarity electrical terminals and a plurality of second polarity electrical terminals, respectively, located on the capacitor body; wherein

each of the first polarity terminals is disposed opposite to another of the first polarity terminals across the capacitor body and each of the second polarity terminals is

disposed opposite to another of the second polarity terminals across the capacitor body; and

at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

2. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to about 1.3 or less.

3. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to about 0.4 or greater.

4. The multi-layer capacitor according to claim 1, wherein the ratio L/W is equal to or less than about 1.3 and greater than or equal to about 0.4.

5. The multi-layer capacitor according to claim 1, wherein the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

6. The multi-layer capacitor according to claim 1, wherein lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

7. The multi-layer capacitor according to claim 1, wherein the lengths L of all of the lead electrodes are substantially equal to each other.

8. The multi-layer capacitor according to claim 1, wherein the capacitor body has a substantially rectangular shape.

9. The multi-layer capacitor according to claim 1, wherein the first polarity terminals and the second polarity terminals are provided only along the opposed side surfaces of the capacitor body.

10. The multi-layer capacitor according to claim 1, wherein at least one of the first polarity terminals is provided at one of the opposed end surfaces and one of the second polarity terminals is provided at another of the opposed end surfaces.

11. The multi-layer capacitor device according to claim 1, wherein the first polarity terminals are disposed opposite to each other across a width of the substantially rectangular capacitor body.

12. The multi-layer capacitor device according to claim 1, wherein the second polarity terminals are disposed opposite to each other across a width of the capacitor body.

13. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals only across a width of the capacitor body.

14. The multi-layer capacitor device according to claim 1, wherein each of the second polarity terminals is disposed opposite to another of the second polarity terminals only across a width of the capacitor body.

15. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals and the corresponding another of the first polarity terminals are located at a common position along a length of the capacitor body.

16. The multi-layer capacitor device according to claim 1, wherein each of the second polarity terminals and the corresponding another of the second polarity terminals are located at a common position along a length of the capacitor body.

17. The multi-layer capacitor device according to claim 1, wherein each of the first polarity terminals is adjacent to one of the second polarity terminals and each of the second polarity terminals is adjacent to one of the first polarity terminals along each of the opposed side surfaces of the capacitor body.

18. The multi-layer capacitor device according to claim 1, wherein the electrical terminals extend to portions of the top and bottom surfaces.

19. The multi-layer capacitor device according to claim 1, wherein none of the first polarity terminals is adjacent to others of the first polarity terminals on the opposed side surfaces of the capacitor body.

20. The multi-layer capacitor device according to claim 1, wherein none of the second polarity terminals is adjacent to others of the second polarity terminals on the opposed side surfaces of the capacitor body.

21. The multi-layer capacitor device according to claim 1, wherein each of the first and second electrode plates includes two of the lead structures extending to each of the pair of opposed side surfaces of the capacitor body.

22. The multi-layer capacitor device according to claim 1, wherein each of the pair of opposed side surfaces of the capacitor body includes at least two of the electrical terminals disposed thereon.

23. The multi-layer capacitor device according to claim 1, wherein each of the pair of opposed side surfaces of the capacitor body includes at least four of the electrical terminals disposed thereon.

24. A multi-layer capacitor according to claim 1, wherein the multi-layer capacitor is arranged to define a decoupling capacitor for a multiprocessing unit.

25. A high frequency circuit comprising at least one multi-layer capacitor according to claim 1.

26. The high frequency circuit according to claim 25, wherein the at least one multi-layer capacitor is arranged to define one of a bypass capacitor and a decoupling capacitor.

27. A wiring substrate comprising at least one multi-layer capacitor according to claim 1 mounted thereon.

28. A multi-layer capacitor device comprising:

a capacitor body including a pair of opposed side surfaces having continuously smooth surfaces and a pair of opposed end surfaces disposed between the pair of opposed side surfaces;

at least four electrical terminals disposed on each of the opposed side surfaces;

the capacitor body also including at least one first electrode plate having a generally substantially rectangular first main electrode portion with a plurality of first lead structures extending therefrom and at least one second electrode plate situated in opposed and spaced apart relation to the first electrode plate, the second electrode plate having a generally substantially rectangular second main electrode portion with a plurality of second lead structures extending therefrom, respective ones of the first lead structures being located adjacent respective ones of the second lead structures in an interdigitated arrangement and extending to respective ones of the electrical terminals;

dielectric material disposed between each opposing set of first and second electrode plates; wherein

each of the lead terminals of the at least one first electrode plate being disposed opposite to another of the lead terminals of the at least one first electrode plate across the capacitor body and each of the lead terminals of the at least one second electrode plate being disposed opposite to another of the lead terminals of the at least one second electrode plate across the capacitor body; and

at least one of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less.

29. The multi-layer capacitor according to claim 28, wherein the ratio L/W is equal to about 1.3 or less.

30. The multi-layer capacitor according to claim 28, wherein the ratio L/W is equal to about 0.4 or greater.

31. The multi-layer capacitor according to claim 28, wherein the ratio L/W is equal to or less than about 1.3 and greater than or equal to about 0.4.

32. The multi-layer capacitor according to claim 28, wherein the width W of at least one of the lead electrodes is different from that of the other lead electrodes.

33. The multi-layer capacitor according to claim 28, wherein lead electrodes are provided on each of a first pair of opposed sides of the capacitor body and a lead electrode is provided on each of a second pair of opposed sides of the capacitor body, and the width W of at least one of the lead electrodes provided on a respective one of the second pair of opposed sides of the capacitor body is wider than the lead electrodes disposed on each of the first pair of opposed sides of the capacitor body.

34. The multi-layer capacitor according to claim 28, wherein the lengths L of all of the lead electrodes are substantially equal to each other.

35. A multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across a width of the substantially rectangular capacitor body.

36. A multi-layer capacitor device according to claim 28, wherein each of the second polarity terminals is disposed opposite to another of the second polarity terminals across a width of the substantially rectangular capacitor body.

37. A multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is disposed opposite to another of the first polarity terminals across a width of the substantially rectangular capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across a width of the substantially rectangular capacitor body.

38. The multi-layer capacitor according to claim 28, wherein the capacitor body has a substantially rectangular shape.

39. The multi-layer capacitor according to claim 28, wherein the first polarity terminals and the second polarity terminals are provided only along the opposed side surfaces of the capacitor body.

40. The multi-layer capacitor according to claim 28, wherein at least one of the first polarity terminals is provided at one of the opposed end surfaces and one of the second polarity terminals is provided at another of the opposed end surfaces.

41. The multi-layer capacitor device according to claim 28, wherein each of the first polarity terminals is adjacent to one of the second polarity terminals and each of the second polarity terminals is adjacent to one of the first polarity terminals along each of the opposed side surfaces of the capacitor body.

42. The multi-layer capacitor device according to claim 28, wherein none of the first polarity terminals is adjacent to others of the first polarity terminals on the opposed side surfaces of the capacitor body.

43. The multi-layer capacitor device according to claim 28, wherein none of the second polarity terminals is adjacent to others of the second polarity terminals on the opposed side surfaces of the capacitor body.

44. The multi-layer capacitor device according to claim 28, wherein each of the first and second electrode plates includes two of the lead structures extending to each of the pair of opposed side surfaces of the capacitor body.

45. The multi-layer capacitor device according to claim 28, wherein each of the pair of opposed side surfaces of the capacitor body includes at least two of the electrical terminals disposed thereon.

46. The multi-layer capacitor device according to claim 28, wherein each of the pair of opposed side surfaces of the capacitor body includes at least four of the electrical terminals disposed thereon.

47. A multi-layer capacitor according to claim 28, wherein the multi-layer capacitor is arranged to define a decoupling capacitor for a multiprocessing unit.

48. A high frequency circuit comprising at least one multi-layer capacitor according to claim 28.

49. The high frequency circuit according to claim 48, wherein the at least one multi-layer capacitor is arranged to define one of a bypass capacitor and a decoupling capacitor.

50. A wiring substrate comprising at least one multi-layer capacitor according to claim 28 mounted thereon.

51. A monolithic capacitor comprising:

a capacitor body having two opposed main surfaces and four side surfaces connected between the two main surfaces, said capacitor body including a plurality of dielectric layers extending in the direction in which the two opposed main surfaces extend, and at least one pair of first and second internal electrodes opposed to each other through one of the dielectric layers so as to define a capacitor unit, said capacitor body further including at least two first lead electrodes extending from one of the first internal electrodes to at least two positions on at least one of the side surfaces, and at least one second lead electrode extending from the second internal electrode to a position located between the positions to which the first lead electrodes extend;

first and second external terminal electrodes provided on the side surfaces onto which the first and second lead electrodes extend, and electrically connected to the first and second lead electrodes, respectively; wherein

the ratio L/W of the length L to the width W of at least one of the first and second lead electrodes is within the range of about 0.4 to about 3.0

52. A monolithic capacitor according to Claim 51, wherein the ratio L/W is in the range of about 0.4 to about 1.3.

53. A monolithic capacitor according to Claim 51, wherein the first and second lead electrodes extend onto at least two of the side surfaces opposed to each other, respectively.

54. A monolithic capacitor according to Claim 51, wherein at least one of the first and second lead electrodes extend onto the respective four side surfaces.

55. A monolithic capacitor according to Claim 51, wherein the first lead electrodes and the second lead electrodes are alternately arranged as viewed in the peripheral directions of the main surfaces.

56. A monolithic capacitor according to Claim 51, wherein the monolithic capacitor is arranged to define a decoupling capacitor connected to a power supply circuit of an MPU chip provided in a microprocessing unit.

57. A wiring substrate including the monolithic capacitor according to Claim 51 mounted thereon.

58. A wiring substrate according to Claim 57, further comprising an MPU chip of a microprocessing unit mounted on the wiring substrate.

59. A decoupling circuit including the monolithic capacitor according to Claim 51.

60. A high frequency circuit including the monolithic capacitor according to Claim 51.

ABSTRACT OF THE DISCLOSURE

A multi-layer capacitor device includes a capacitor body including top and bottom surfaces and opposed side surfaces which have continuously flat surfaces and are disposed between the top and bottom surfaces and opposed end surfaces disposed between the top and bottom surfaces and the opposed side surfaces. The capacitor body includes a plurality of first electrode plates and a plurality of second electrode plates. The first and second electrode plates are interleaved with each other in opposed and spaced apart relation. A dielectric material is located between each opposed set of the first and second electrode plates. The first and second electrode plates each include a main electrode portion and a plurality of spaced apart lead structures extending therefrom. Respective lead structures of the first electrodes plates are located adjacent respective lead structures of the second electrode plates in an interdigitated arrangement. A plurality of electrical terminals are located on each of the opposed side surfaces of the capacitor body, corresponding lead structures of the first electrode plates and corresponding lead structures of the second electrode plates being electrically connected together by respective ones of the electrical terminals to define a plurality of first polarity electrical terminals and a plurality of second polarity electrical terminals, respectively, located on the capacitor body. Each of the first polarity terminals is disposed opposite to another of the first polarity terminals across the capacitor body and each of the second polarity terminals is disposed opposite to another of the second polarity terminals across the capacitor body. Each of the lead structures of the first and second electrode plates have a length L and a width W and a ratio L/W is equal to about 3 or less, and preferably between 0.4 and 1.3.

FIG. 1

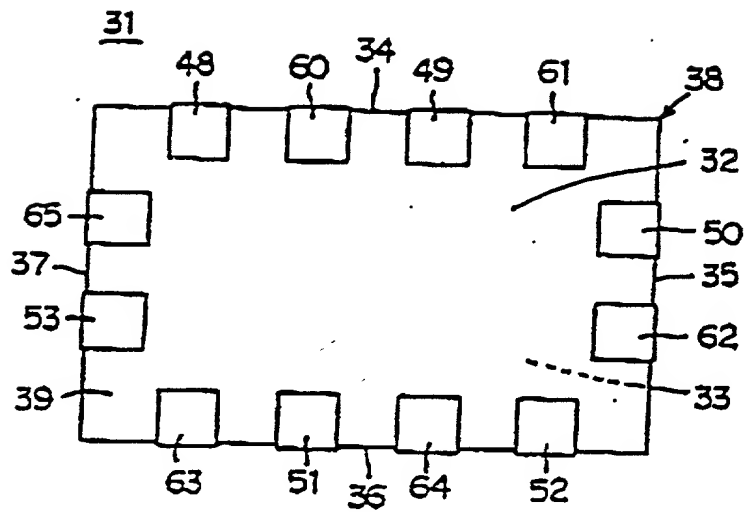
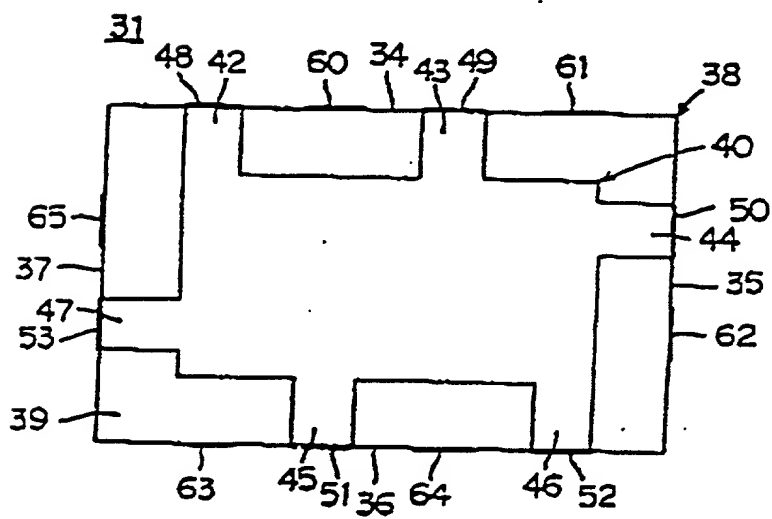


FIG. 2



000000-000000-000000

FIG. 3

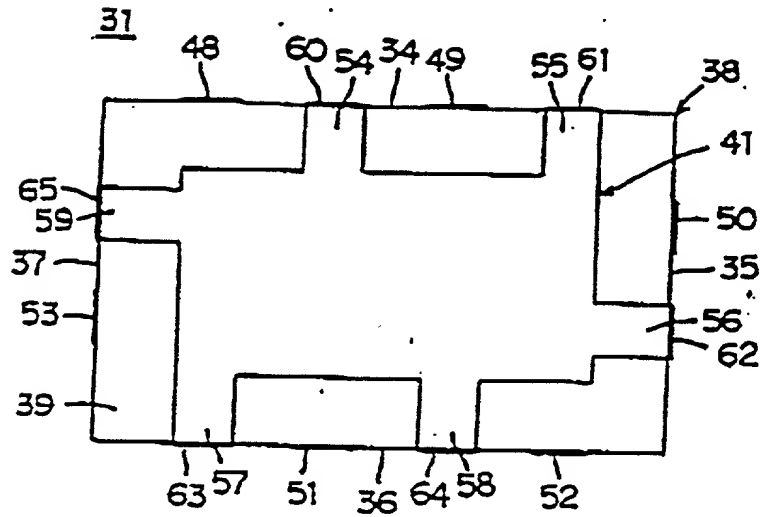


FIG. 4

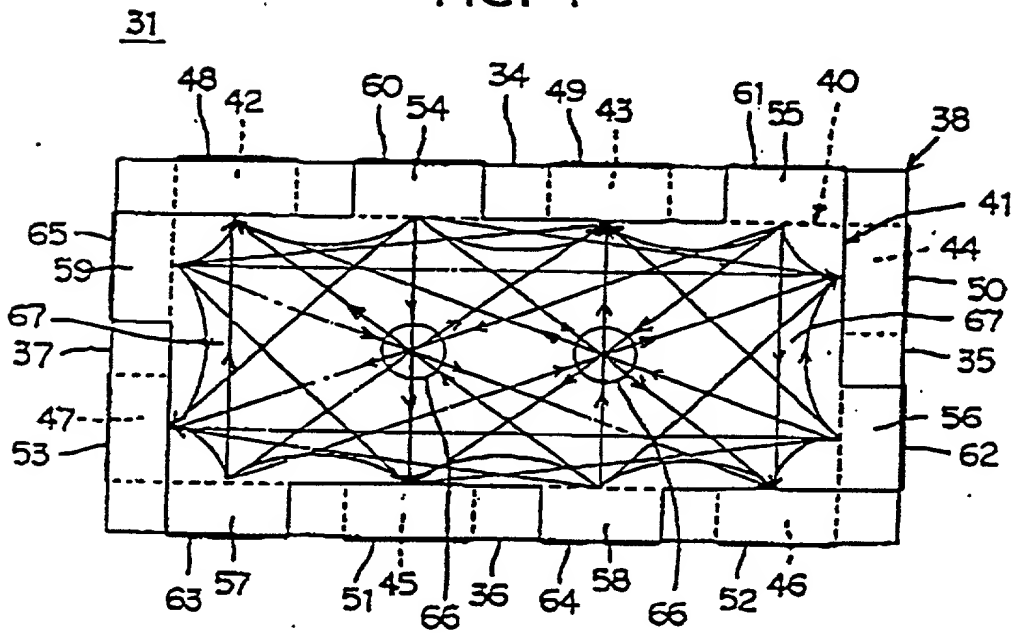


FIG. 5

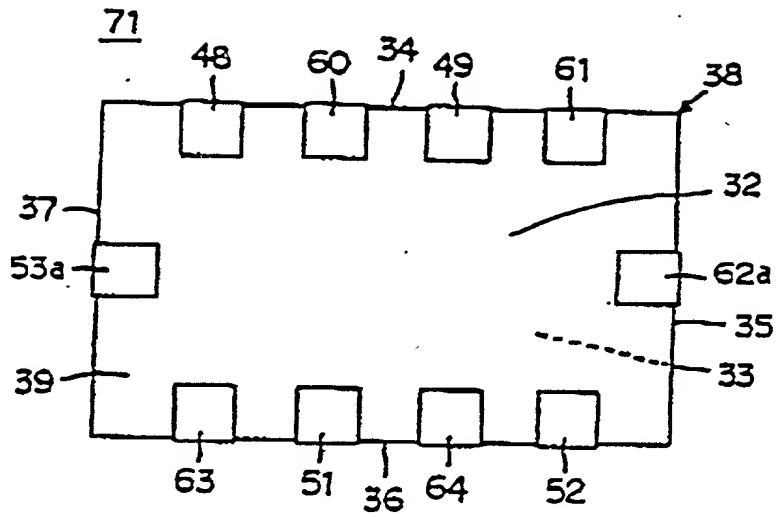


FIG. 6

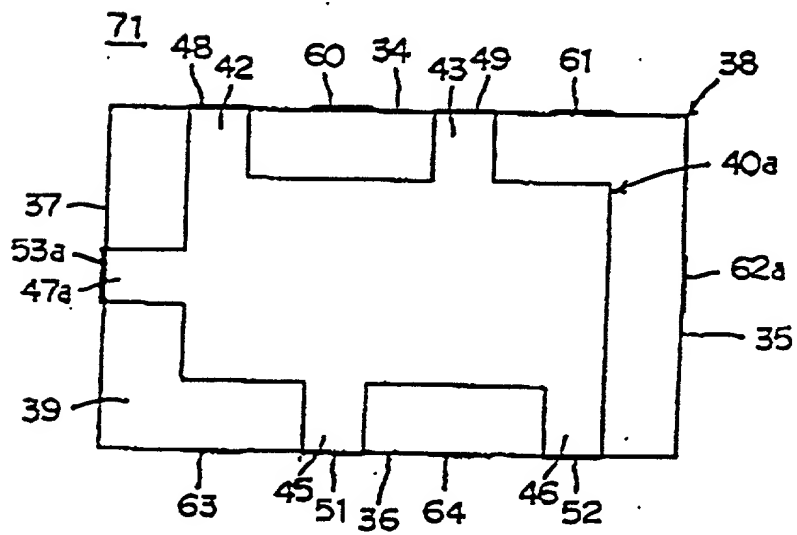


FIG. 7

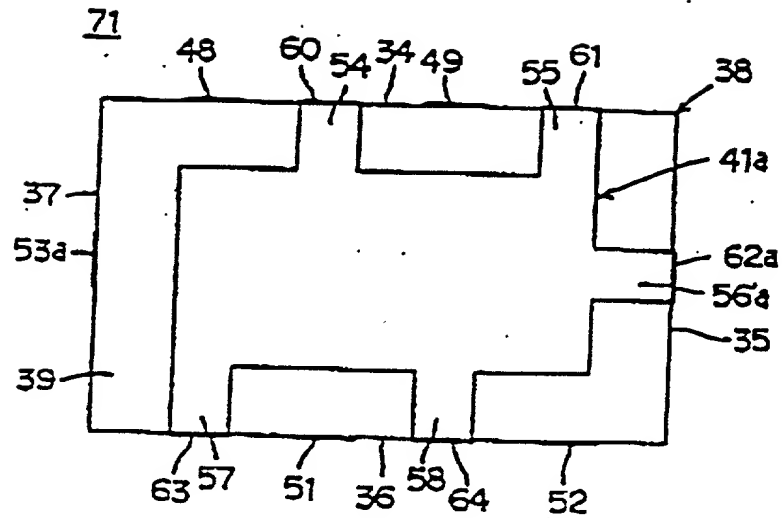


FIG. 8

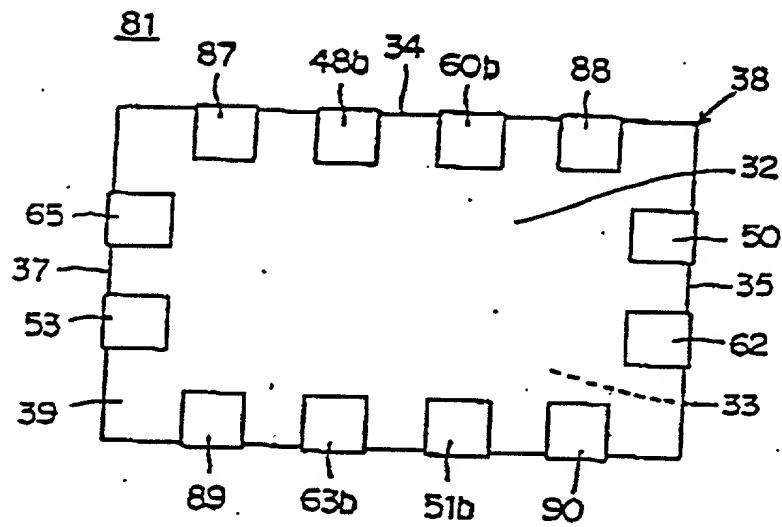


FIG. 9

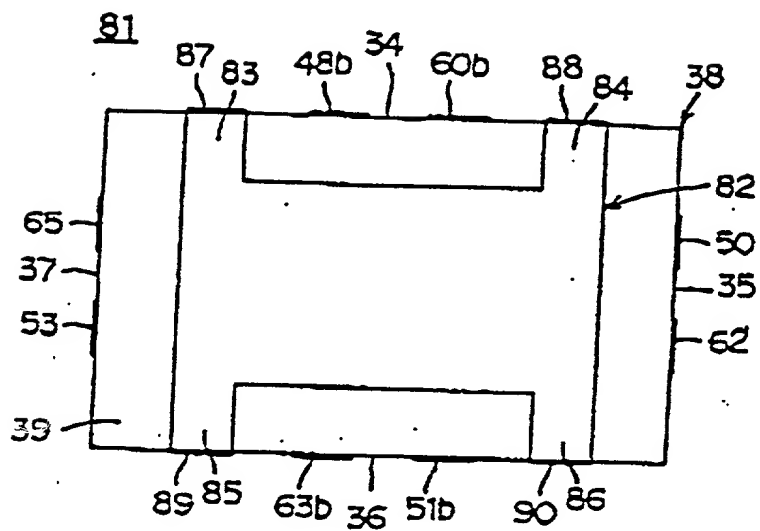
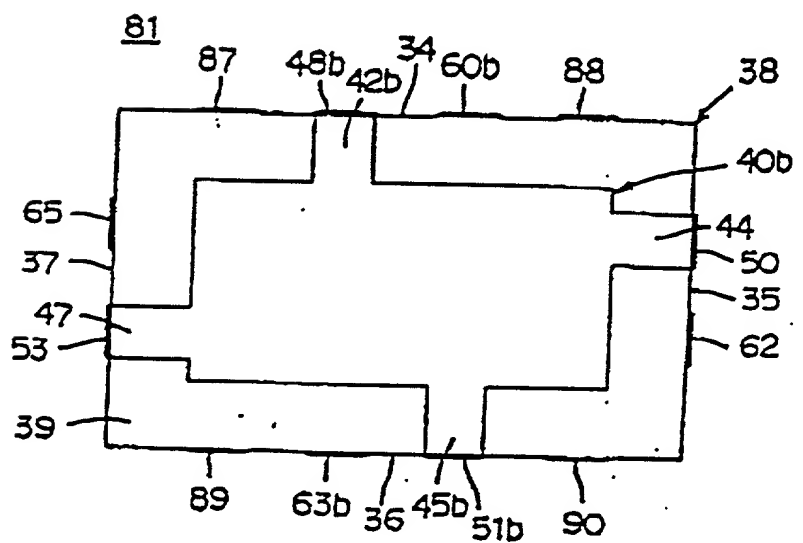
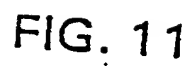


FIG. 10





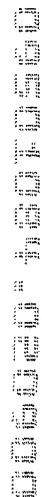
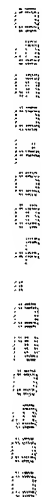
[illegible][illegible]

FIG. 15
PRIOR ART

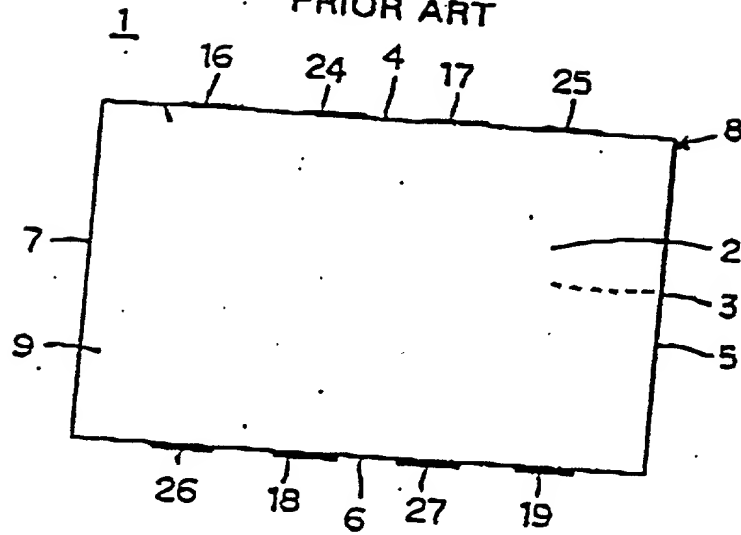


FIG. 16
PRIOR ART

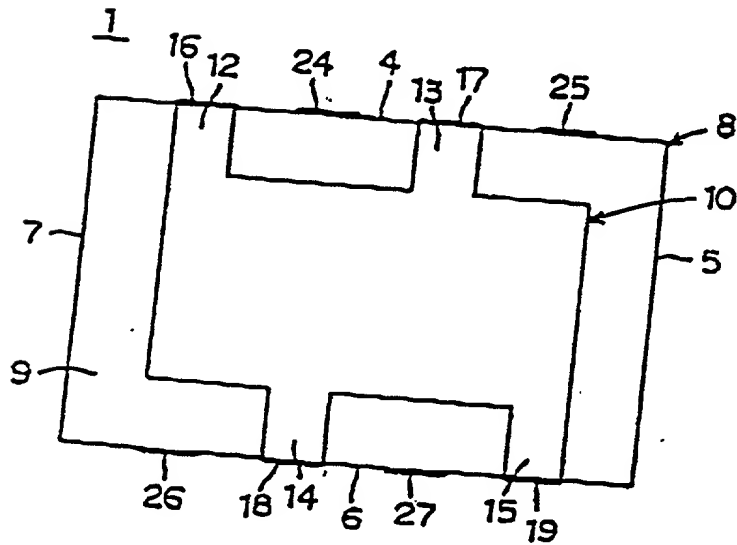


FIG. 17
PRIOR ART

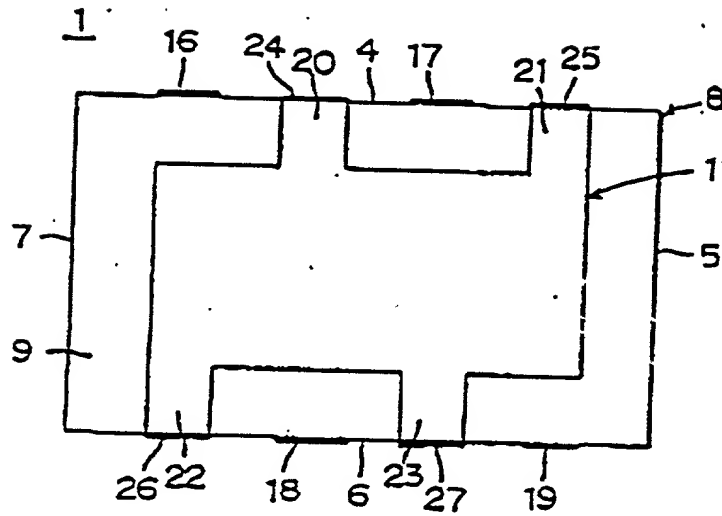
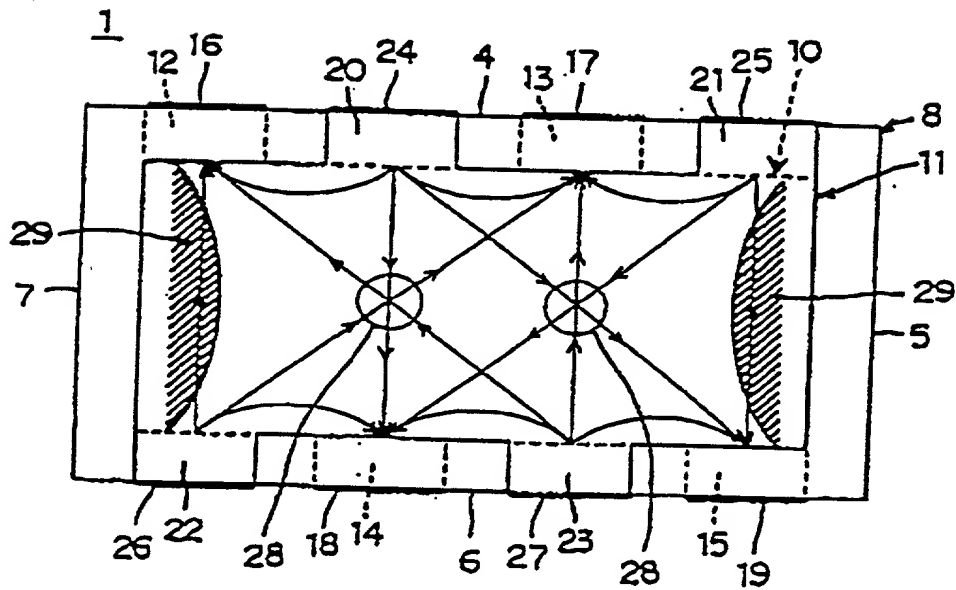
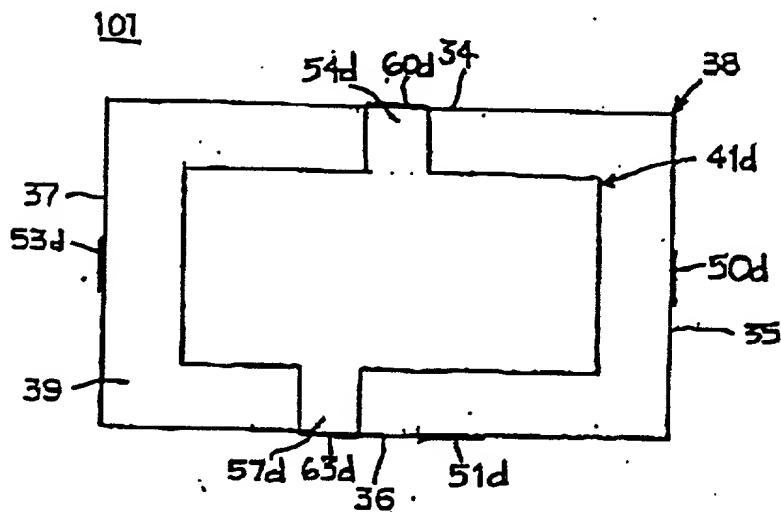
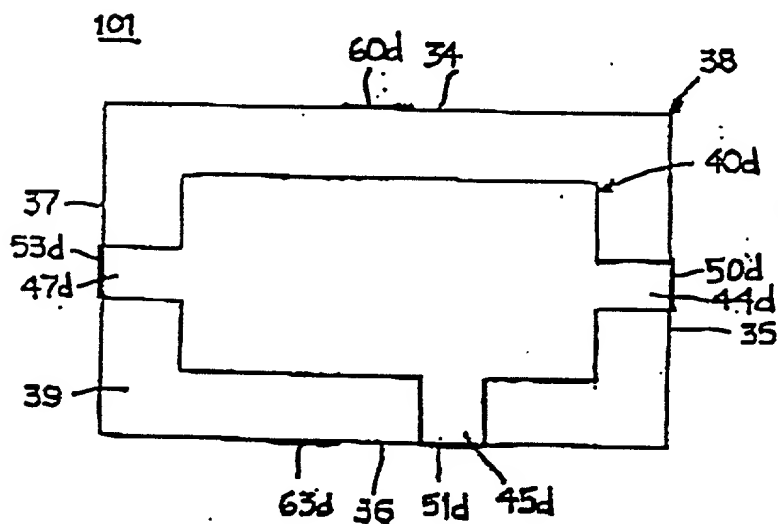
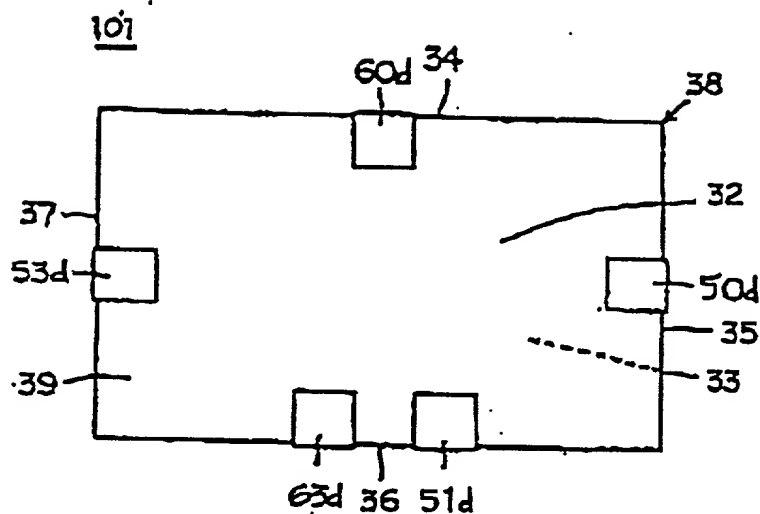


FIG. 18
PRIOR ART





Attorney Docket No. 36856.260

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled MULTILAYER CAPACITOR the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number on _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)	Priority Date	Priority Claimed
9-306717 (Number)	JAPAN (Country) (PCT)	November 10, 1997 (Day/Month/Year Filed)
		Yes No <input checked="" type="checkbox"/> <input type="checkbox"/>
11-370803 (Number)	JAPAN (Country) (PCT)	December 27, 1999 (Day/Month/Year Filed)
		Yes No <input checked="" type="checkbox"/> <input type="checkbox"/>

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

(Application Number)	(Filing Date)	(Status -- patented, pending, abandoned)
09/042,379	March 13, 1998	Pending

(Application Number)

(Filing Date)

(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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